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| **EC-5263** | **Advanced CMOS Devices And Technology** | **L T P C** |
|  | M.Tech. (MVD), Second Semester (Elective – III) | 3 0 0 3 |

**FUNDAMENTALS**

History of Si technology, Review of CMOS scaling. Problems with traditional geometric scaling. Power crisis. Review of basic quantum mechanics. Mobility enhancement techniques. Review of stress and strain, how it affects band structure of silicon. Types and realization of stress elements. Problems with stress elements. L1-L5

**HIGH-κ GATE DIELECTRIC AND PROCESS**

Gate oxide scaling trend. Urgency to switch gate dielectric material. High K material selection. Fermi level pinning Process integration of high K gate dielectrics and metal gates Multi-gate transistors. Ways of realization. Fabrication issues and integration challenges. L6-L13

**CMOS COMPATIBLE MEMORY DEVICES**

SRAM, DRAM, Flash Memories (FG and CT), Emerging Memories (FeRAM, MRAM, ReRAM, PCRAM) L14-17

**SOI DEVICES**

Basic principle of MOSFETs, Introduction to classical planer bulk MOSFETs, VMOS devices. Introduction to SOI Technology, radiation hardness capability. Partially depleted SOI MOSFET, Fully depleted SOI MOSFET. Single gate SOI MOSFET, Double Gate SOI MOSFET, kink effect, Floating Body effect, Applications of SOI MOSFET, Comparison with Classical planer bulk MOSFET. L18-24

**MULTIGATE CMOS DEVICES**

Introduction to Finfets, Ways of realization, Fabrication issues and integration challenges. L25-30   
**Analog, Digital Models and Layout Dependent Effects**

Analog and digital benchmarking of models. Layout dependent effects. Test structures used for characterization, Variations and how it can affect scaling. Basics of sub wavelength lithography. Design for manufacturability. L31-37

**References:**

1. Hei Wong, “Nano-CMOS Gate Dielectric Engineering,” CRC, 2011.
2. J.P. Colinge, “FinFETs and Other Multi-Gate Transistors,” Springer, 2010.
3. B. Wong, A. Mittal, Y. Cao, G. Starr, “Nano-CMOS Circuit and Physical Design”, Wiley Inter-science 2004.
4. A. Dimoulas, E. Gusev, P. McIntyre, M. Heyns, "Advanced Gate Stacks for High-Mobility Semiconductors", Springer 2007.

**COs:**

The students will be able to

1. Understand the scaling rules, power crisis.
2. Analyse the impact of gate oxide scaling issues of the devices
3. Demonstrate the SOI device Technology considering fully depleted and partially depleted case
4. Illustrate the multigate device physics
5. Apply the concept of benchmarking analog and digital models and layouting

CO-PO mapping

|  |  |  |  |  |  |  |
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| POs  COs | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
| CO1 | \* |  |  |  |  |  |
| CO2 | \* | \* | \* | \* | \* |  |
| CO3 | \* | \* | \* | \* | \* |  |
| CO4 | \* | \* | \* | \* | \* |  |
| CO5 |  | \* | \* |  |  |  |